

Fig. 1

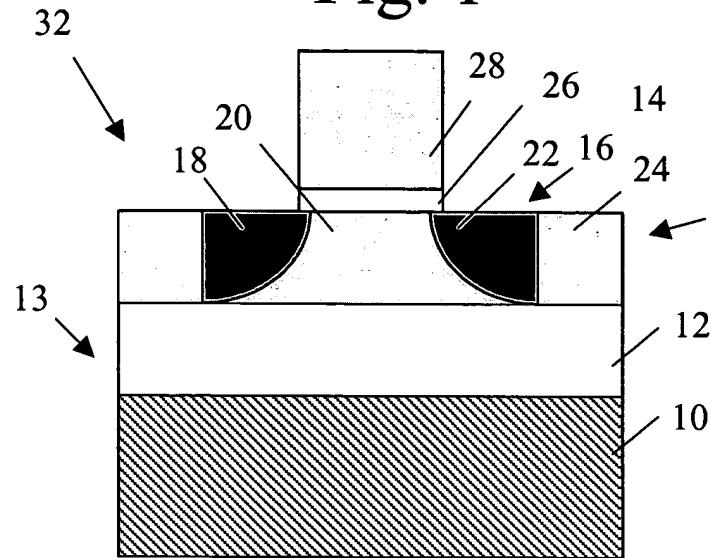


Fig. 2

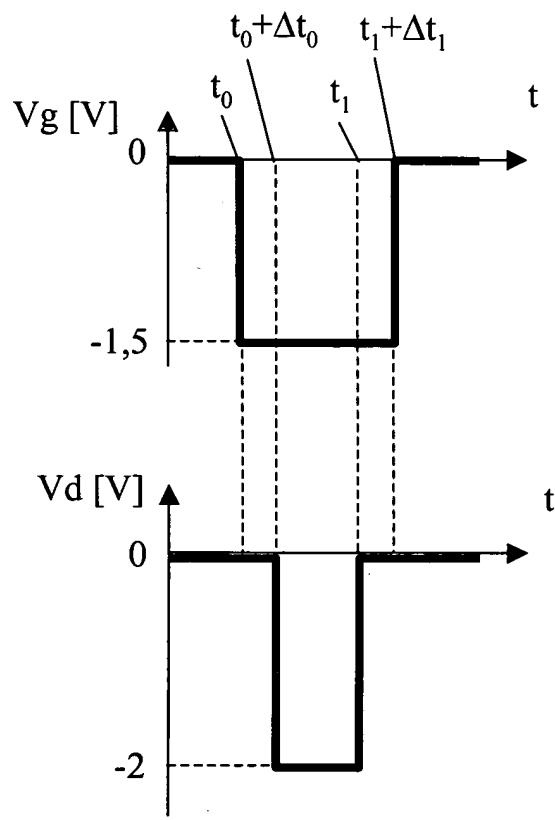


Fig. 3

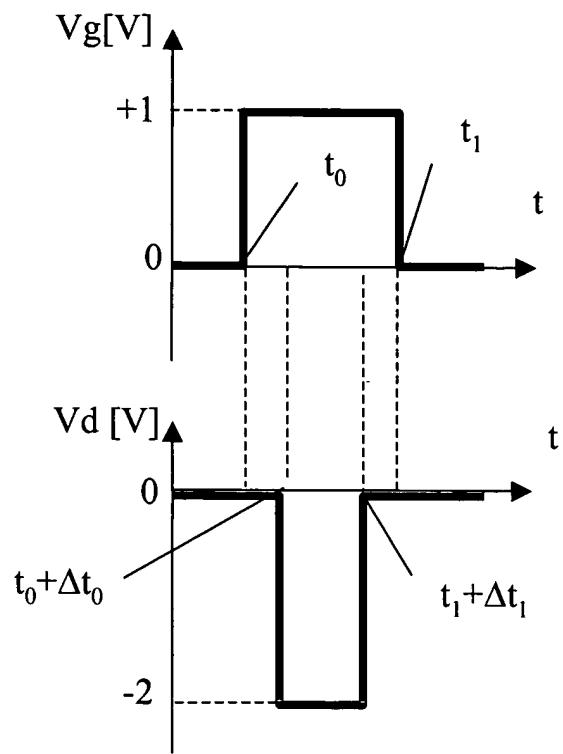


Fig. 4

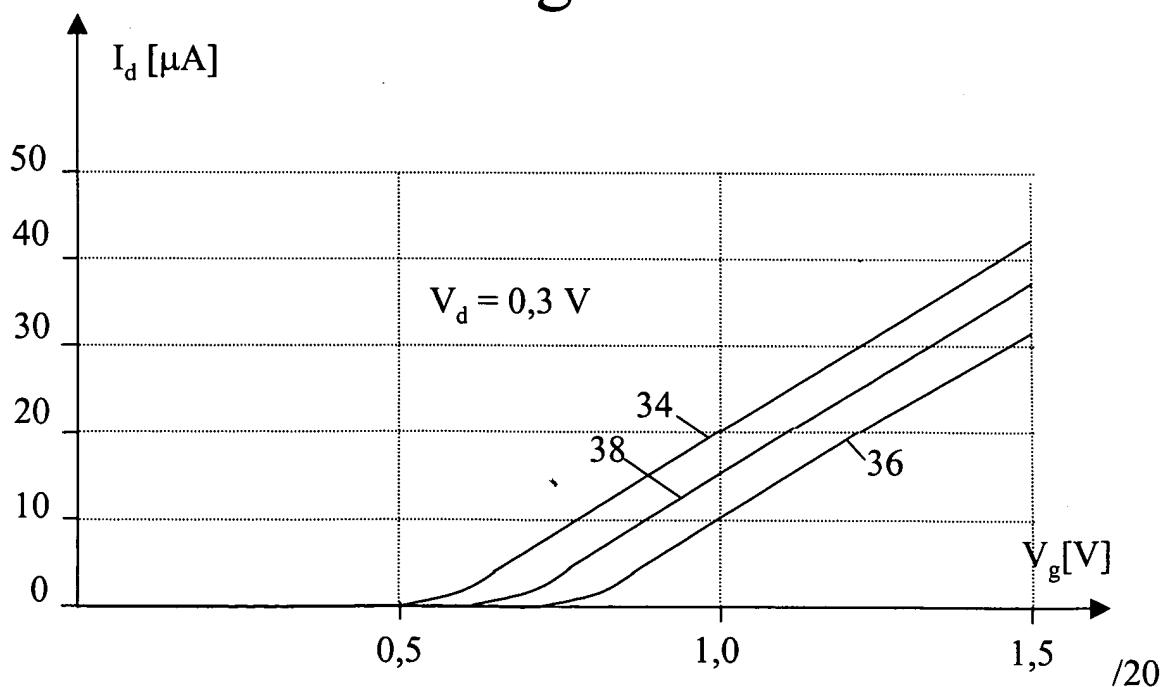


Fig. 5b

Fig. 5a

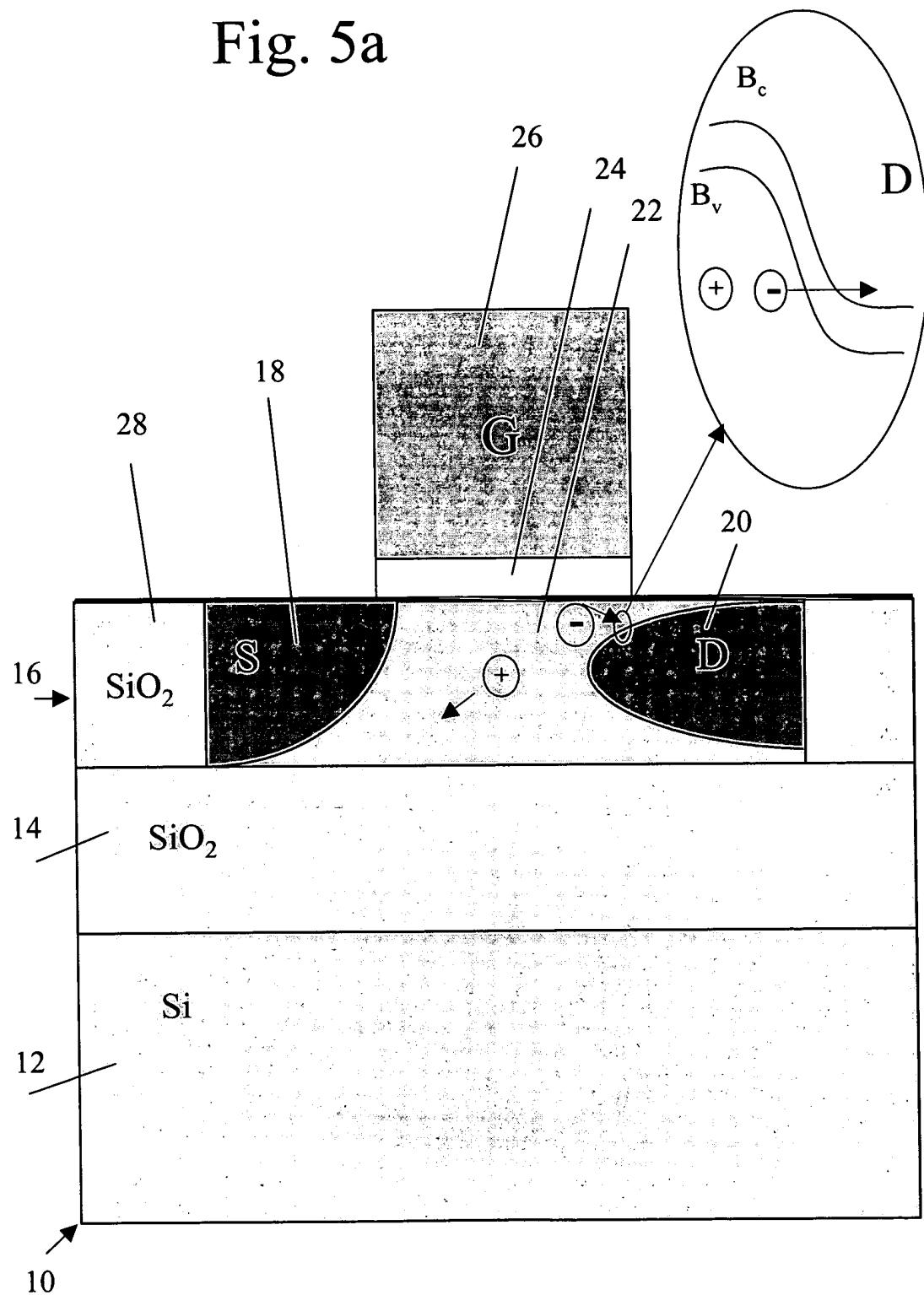


Fig. 6a

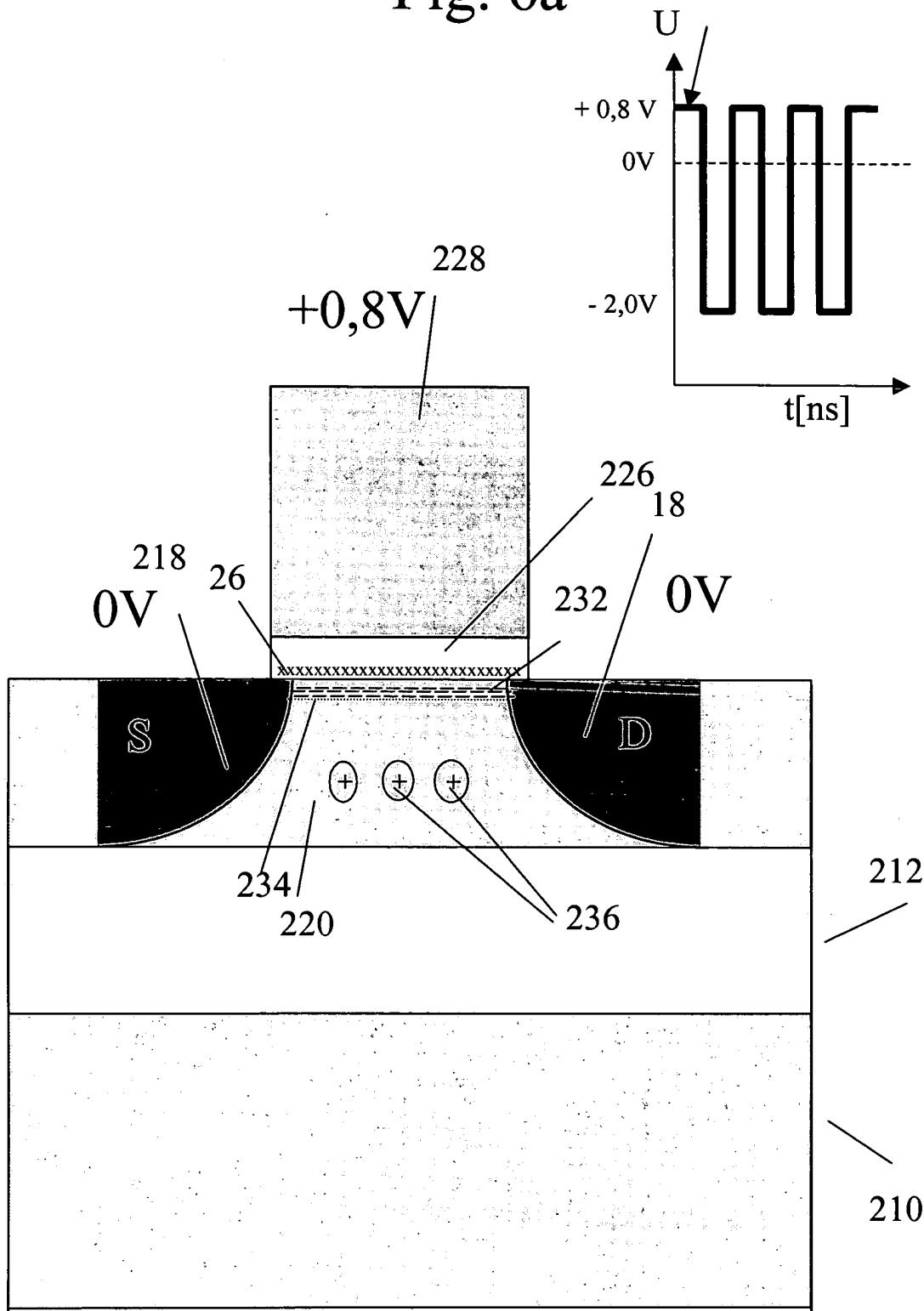


Fig. 6b

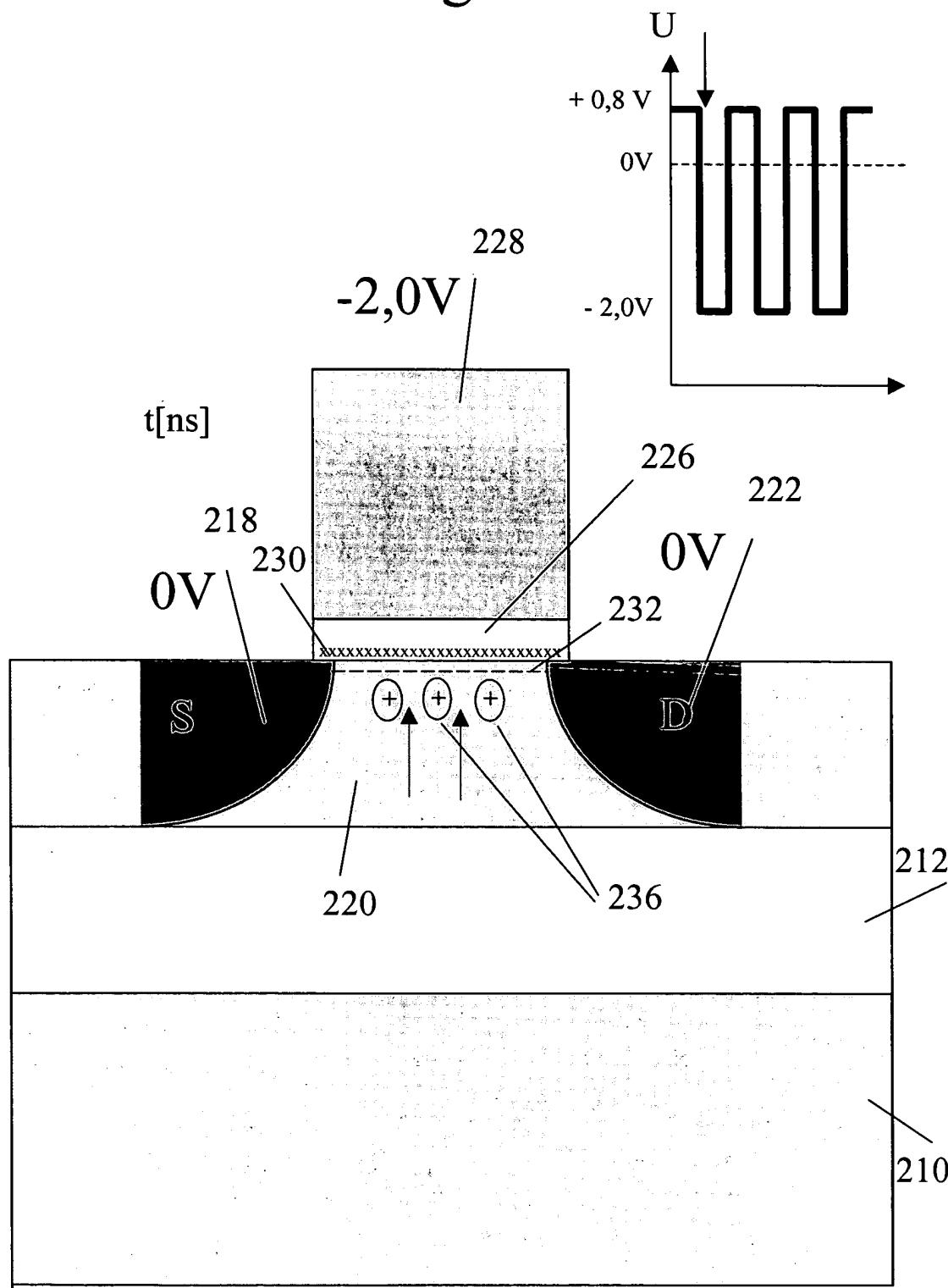


Fig. 6c

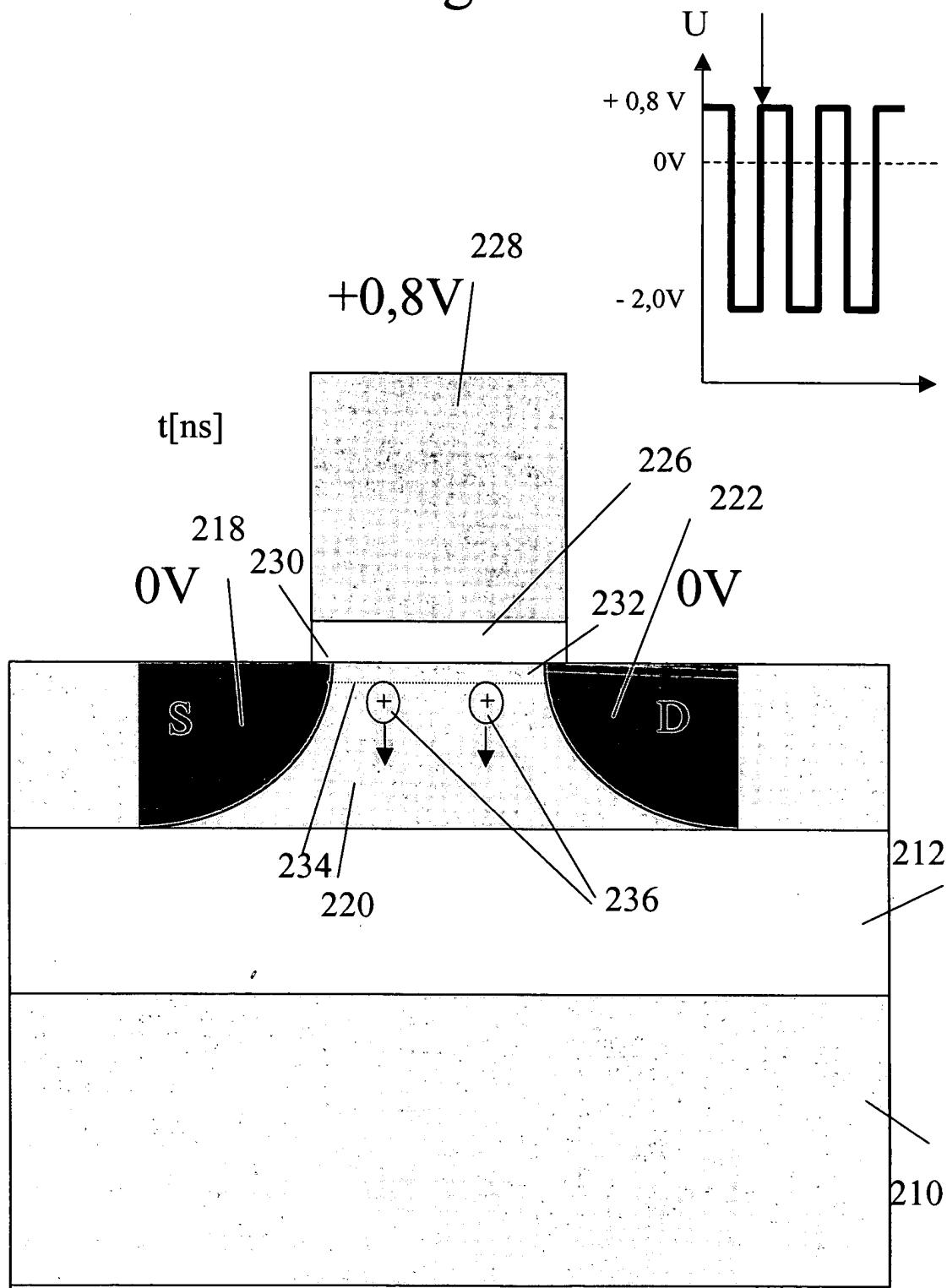


Fig. 7a

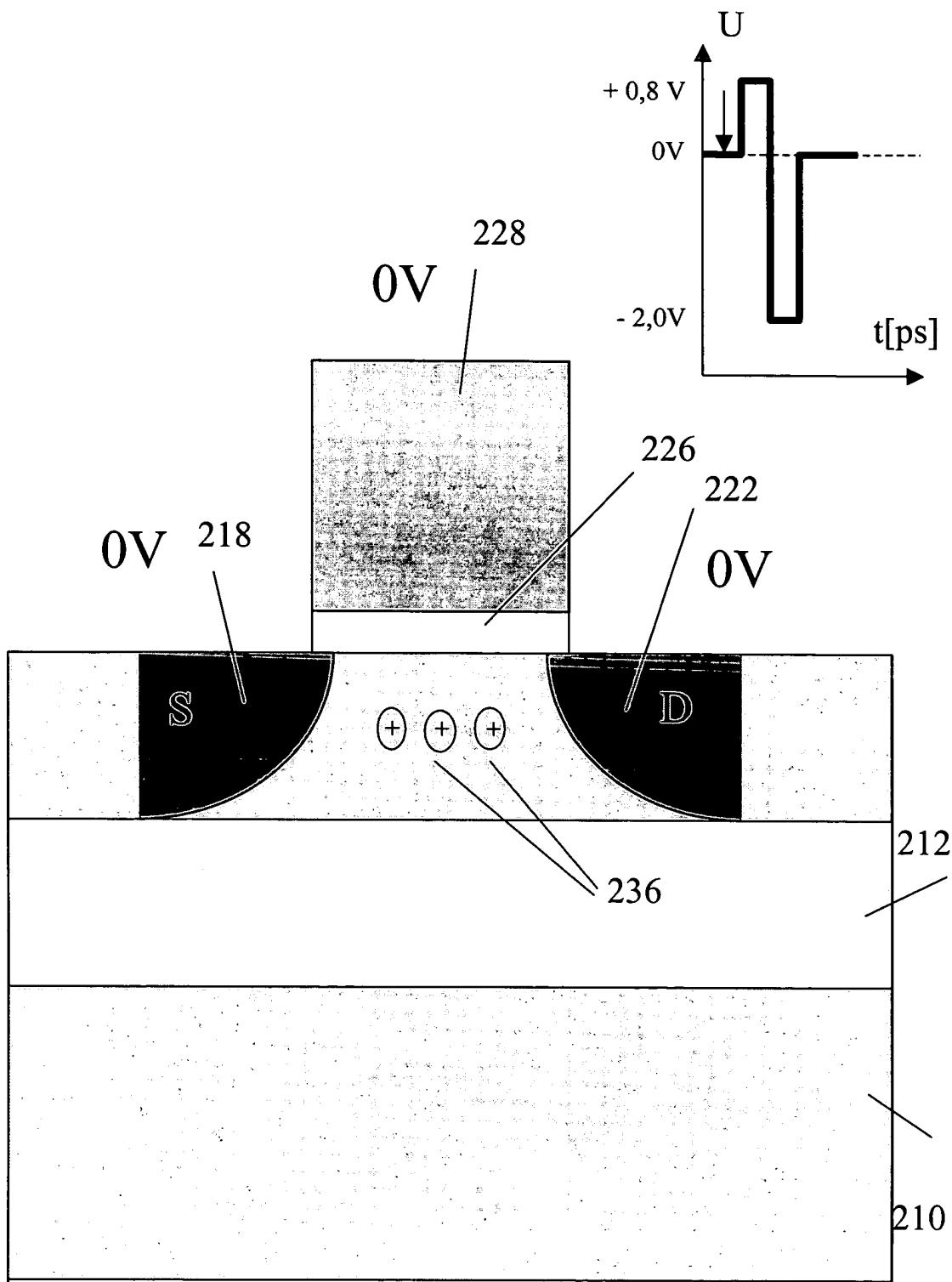


Fig. 7b

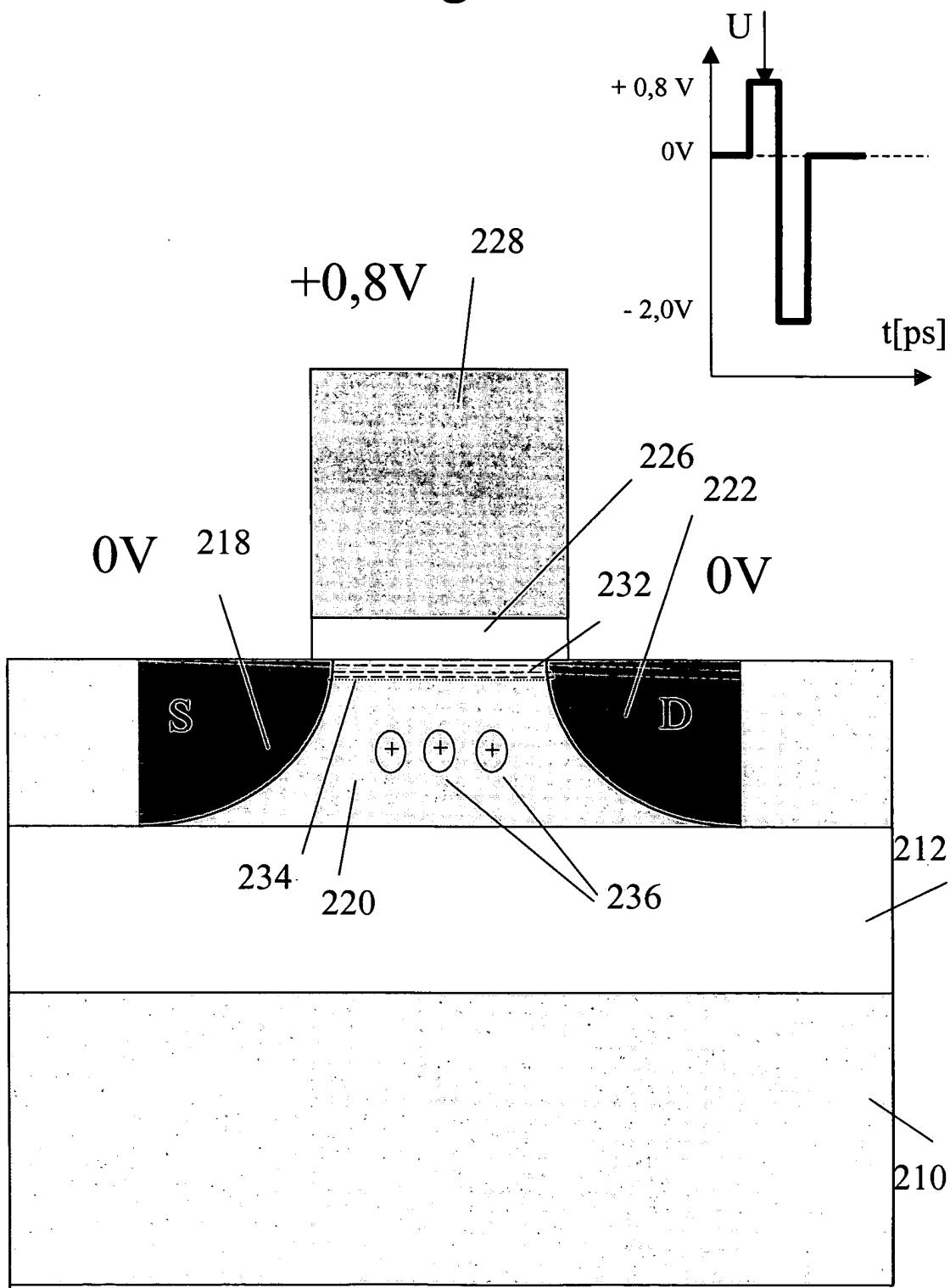


Fig. 7c

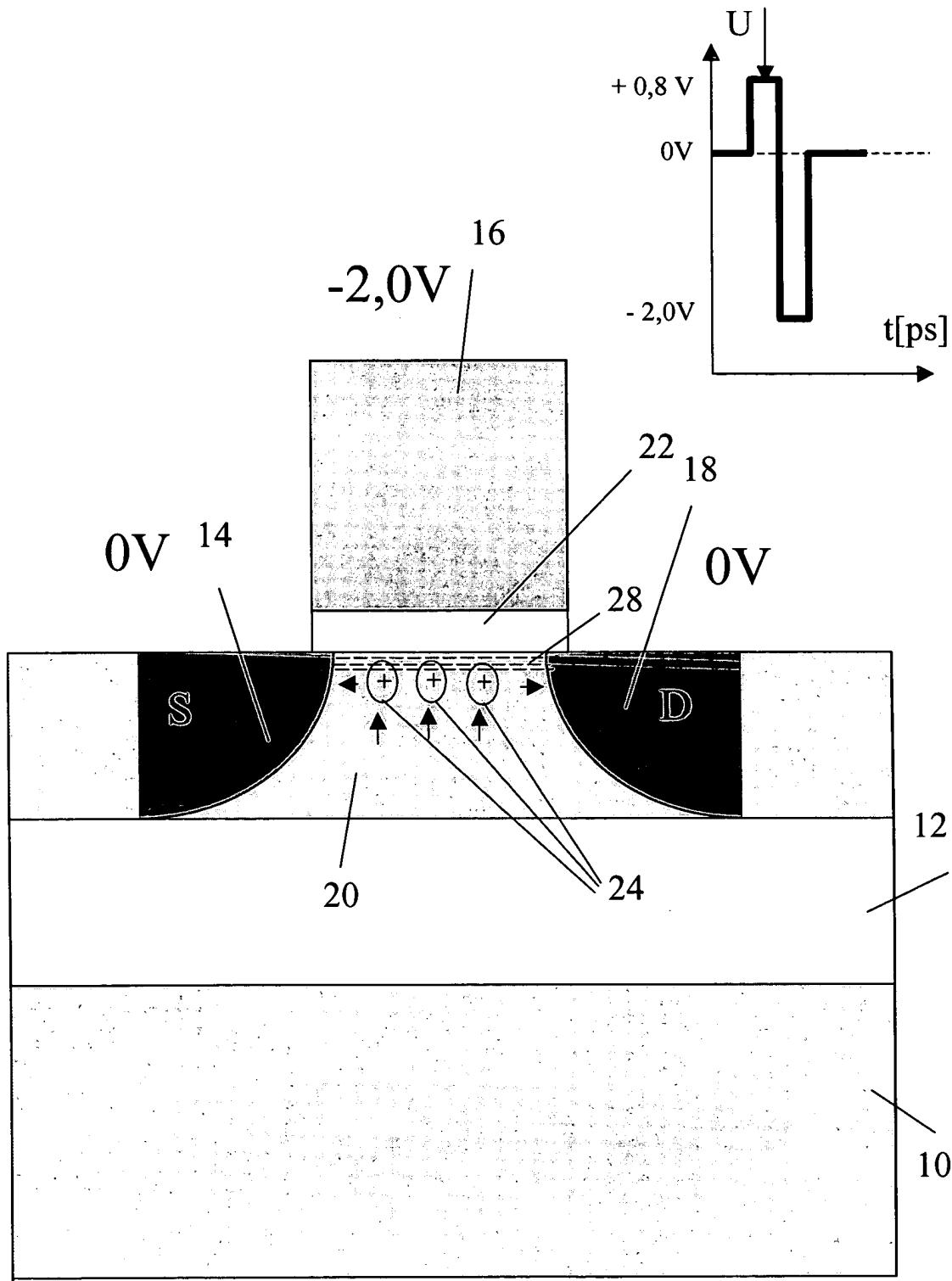


Fig. 7d

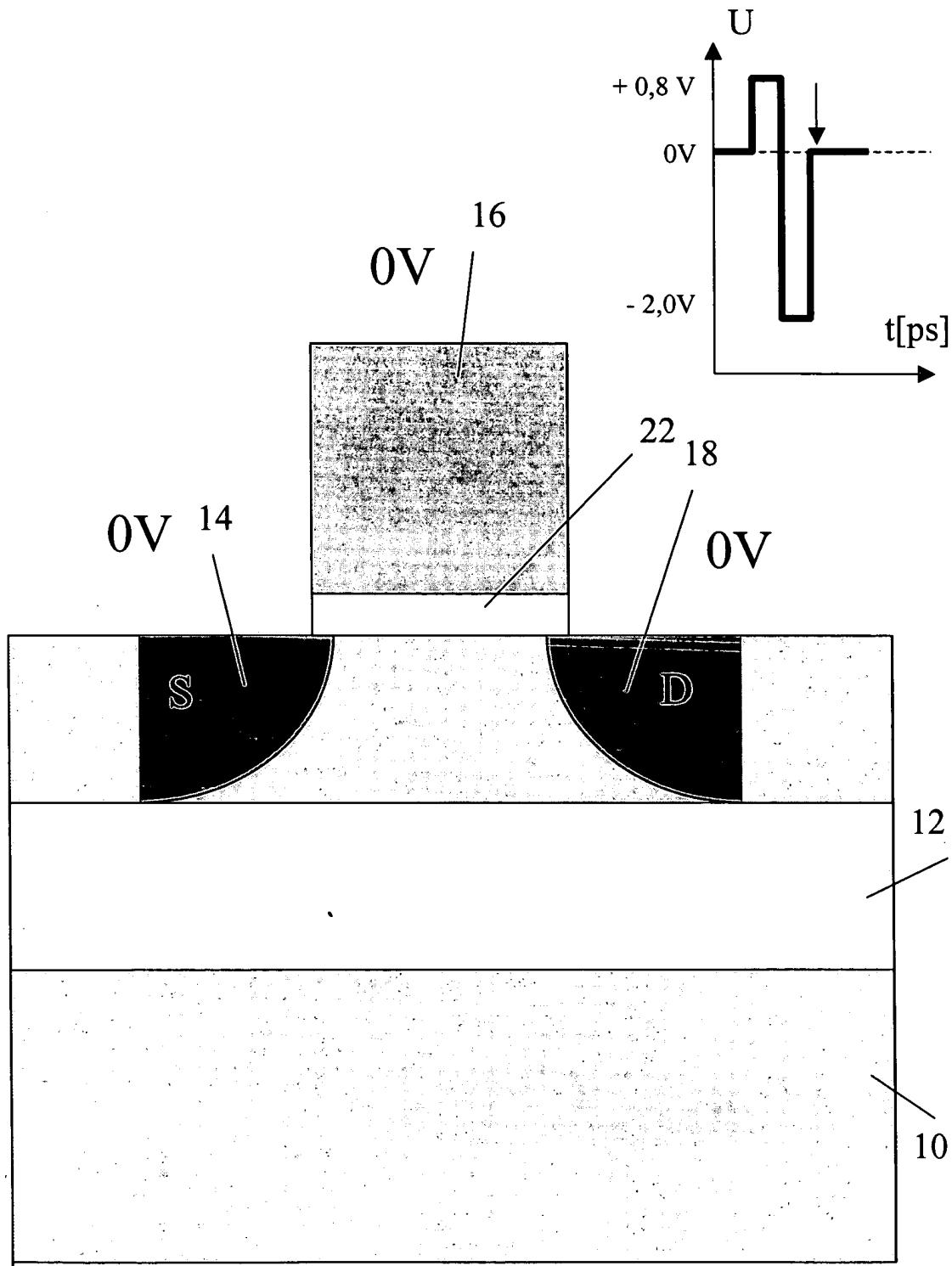


Fig. 8

**PD-SOI
NMOS**

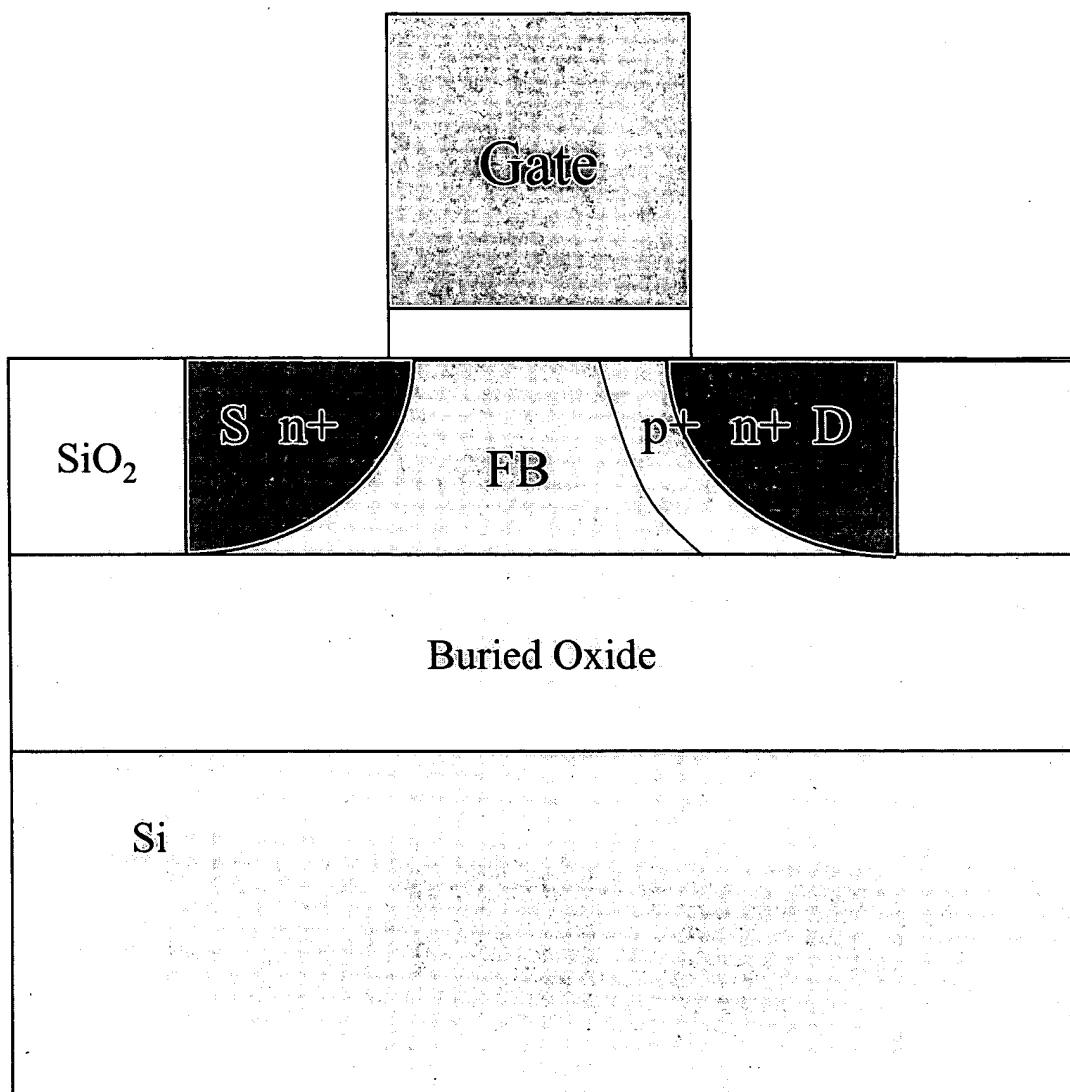


Fig. 9

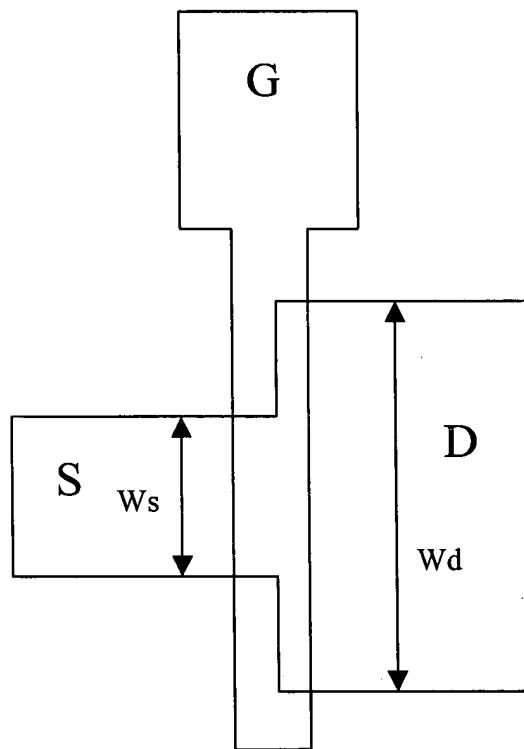
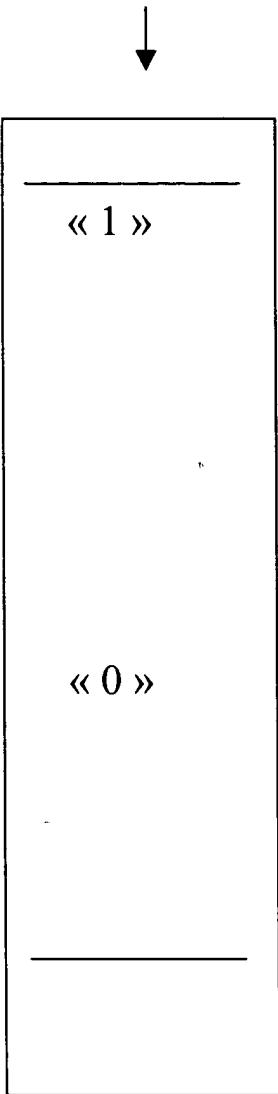
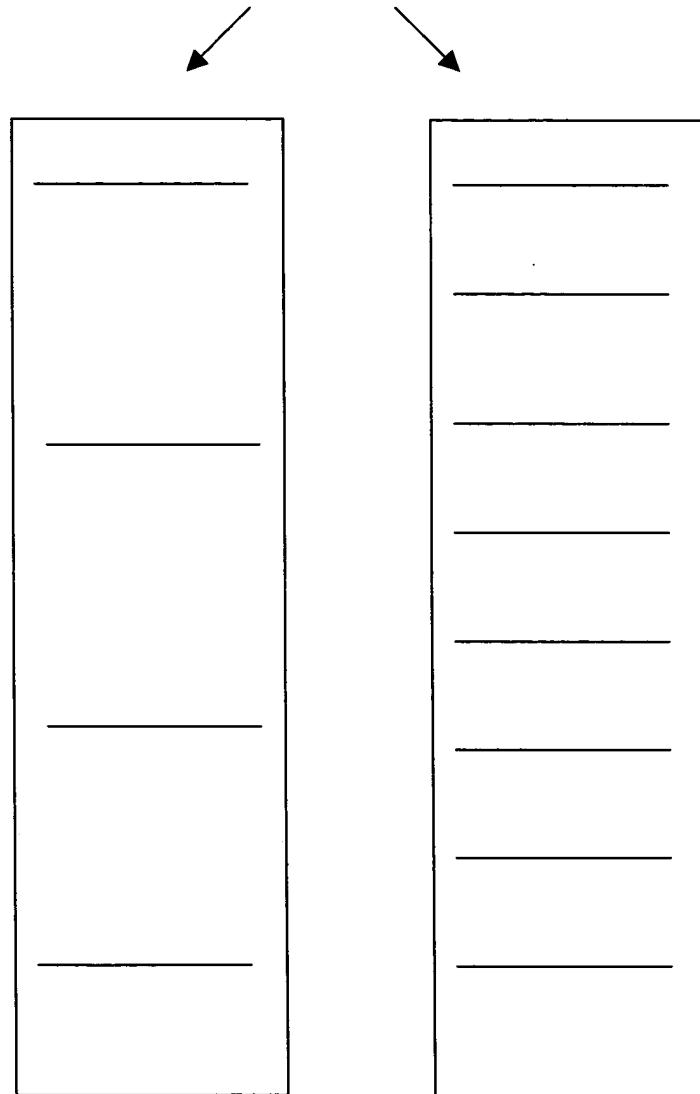


Fig. 10

Binary memory



Multilevel memory



a)

b)

c)

Fig. 11

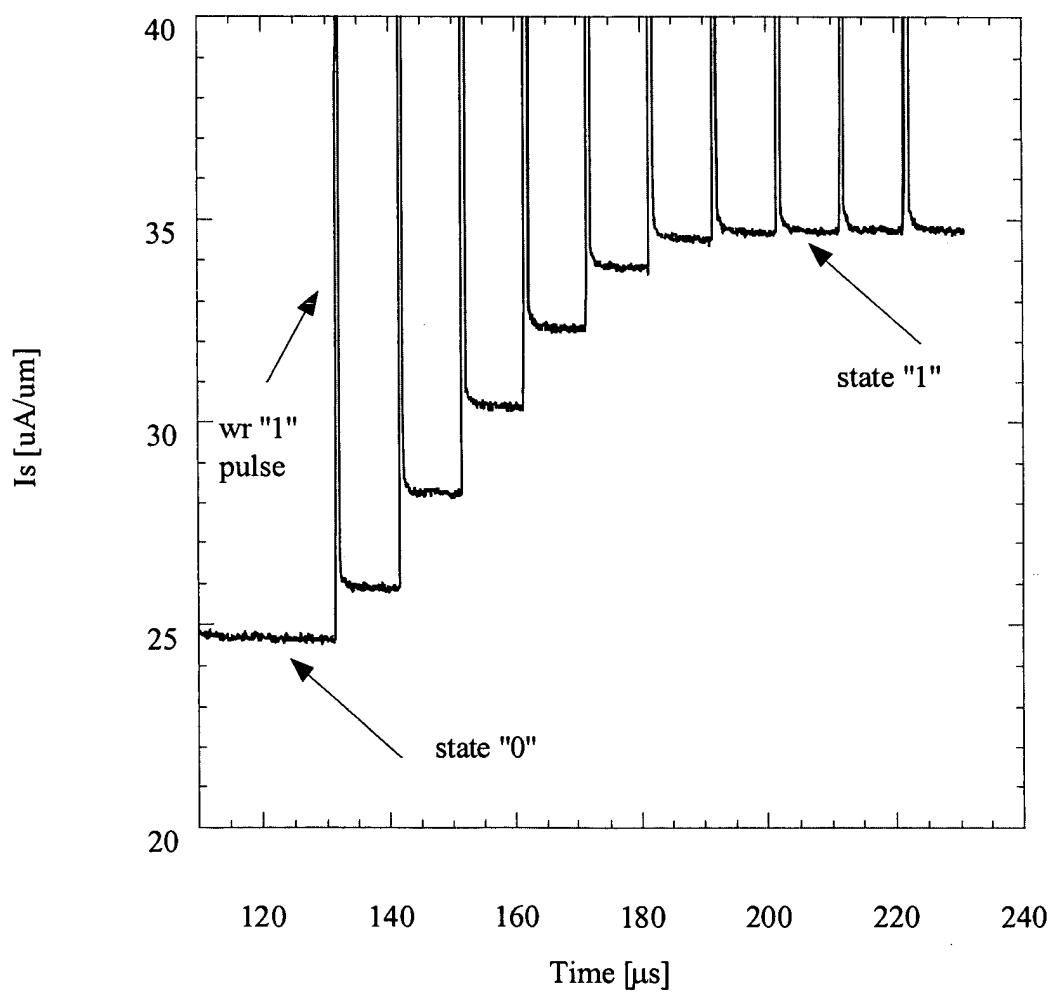


Fig. 12

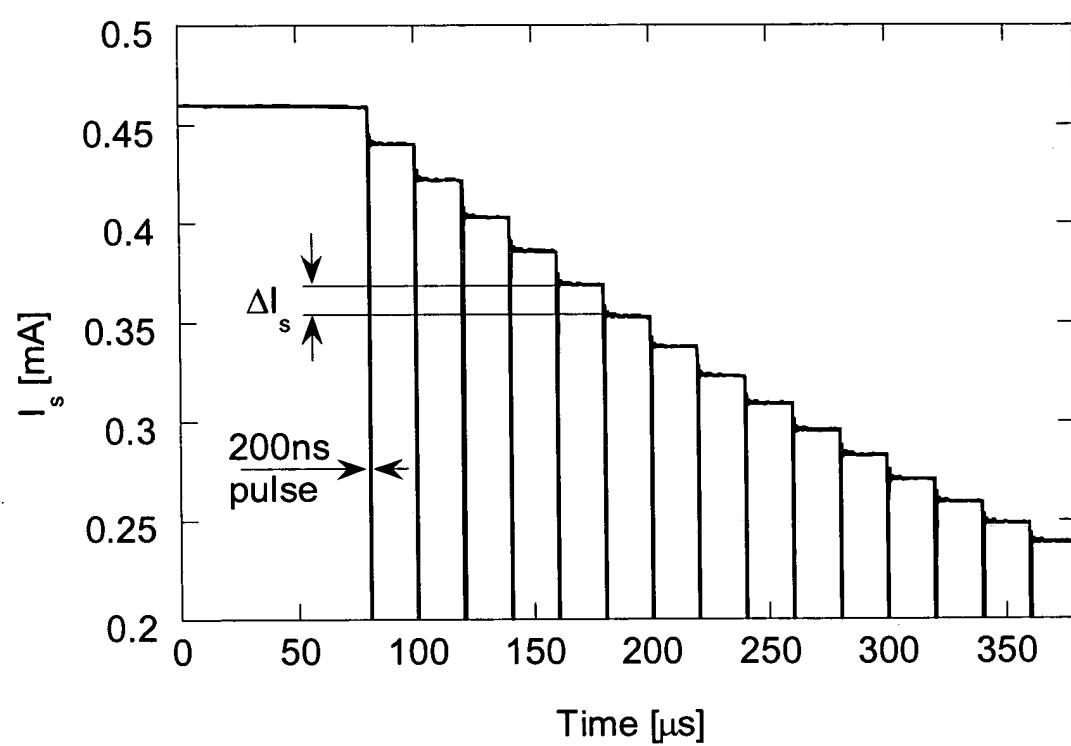


Fig. 13

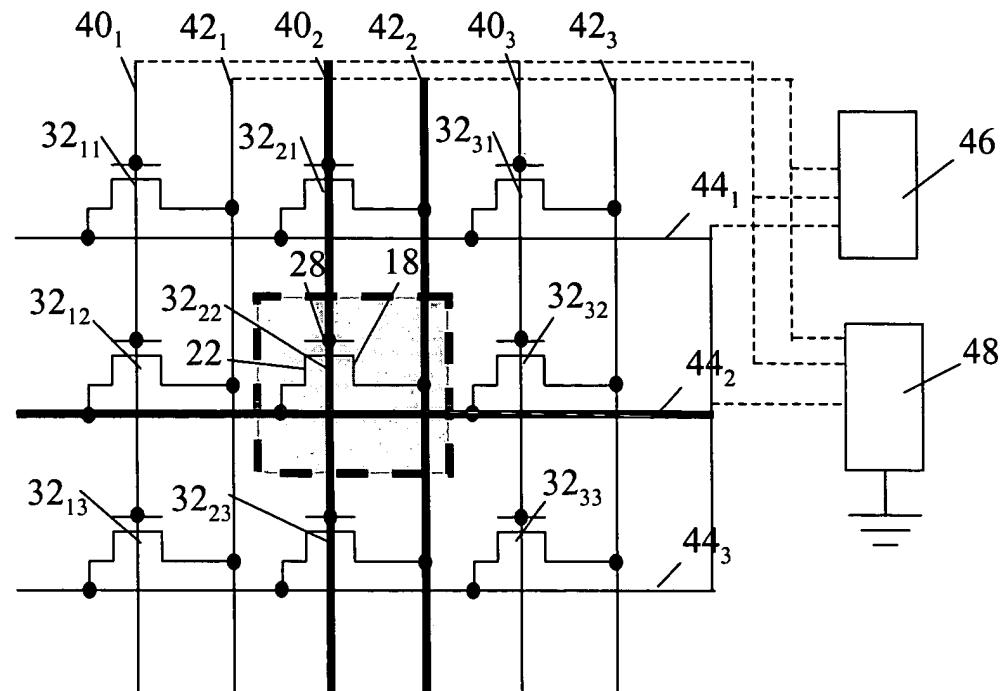


Fig. 14

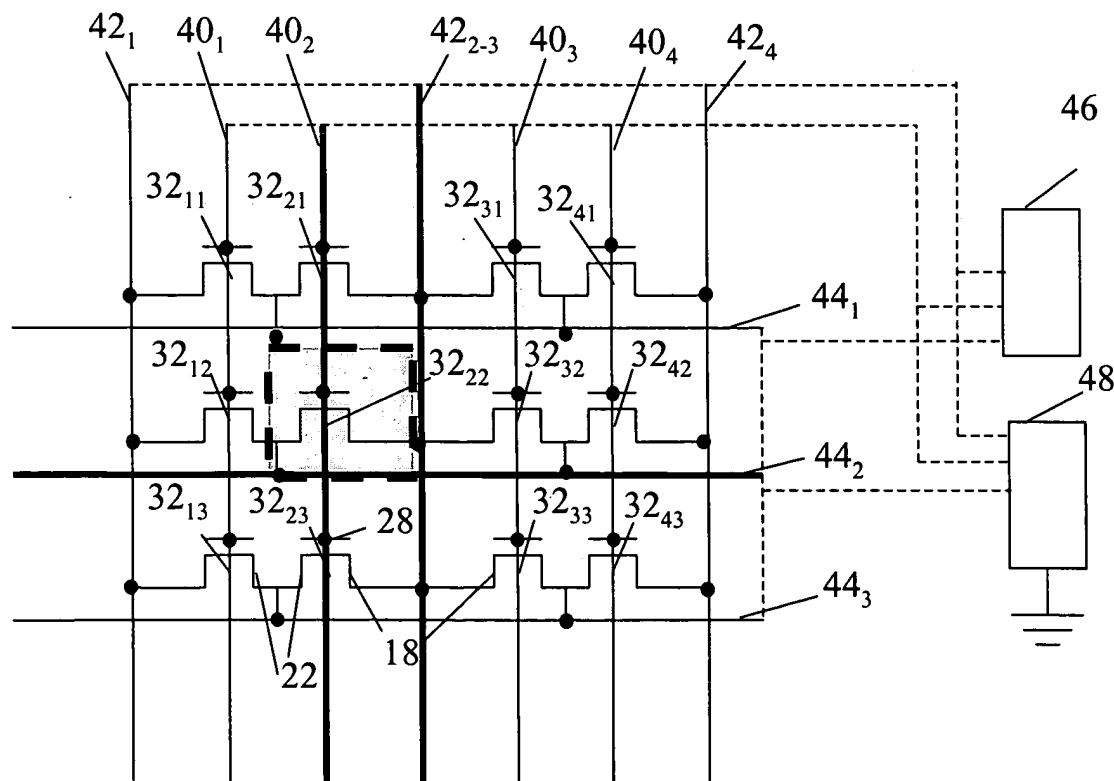


Fig. 15

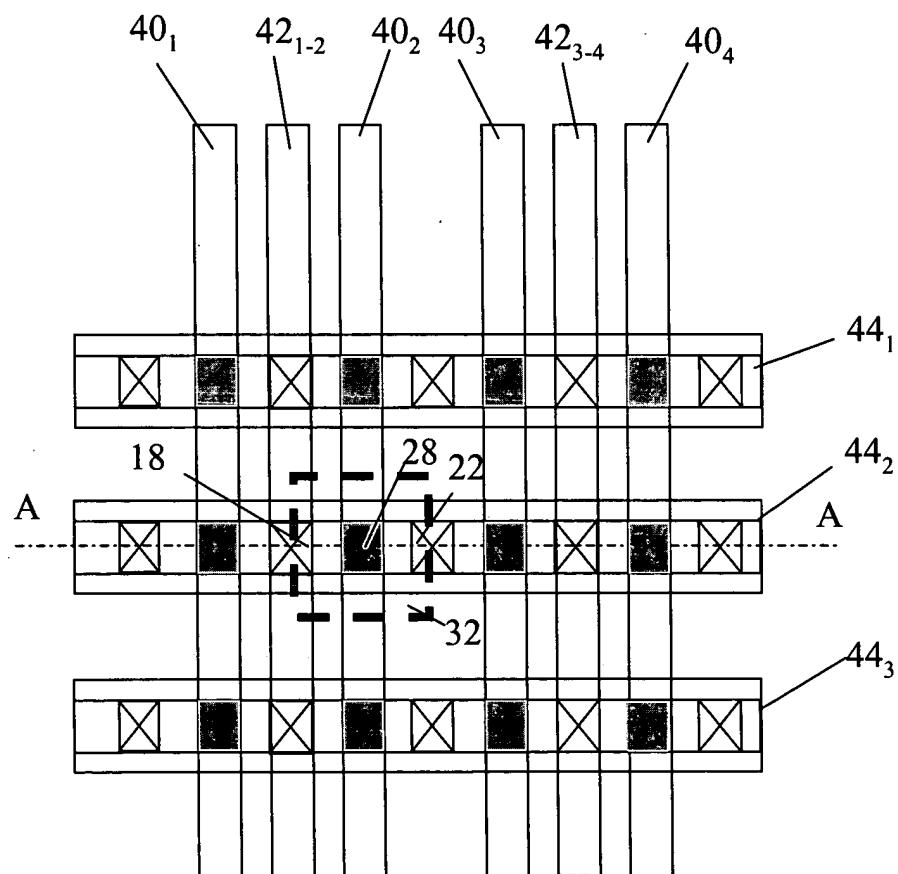


Fig. 16

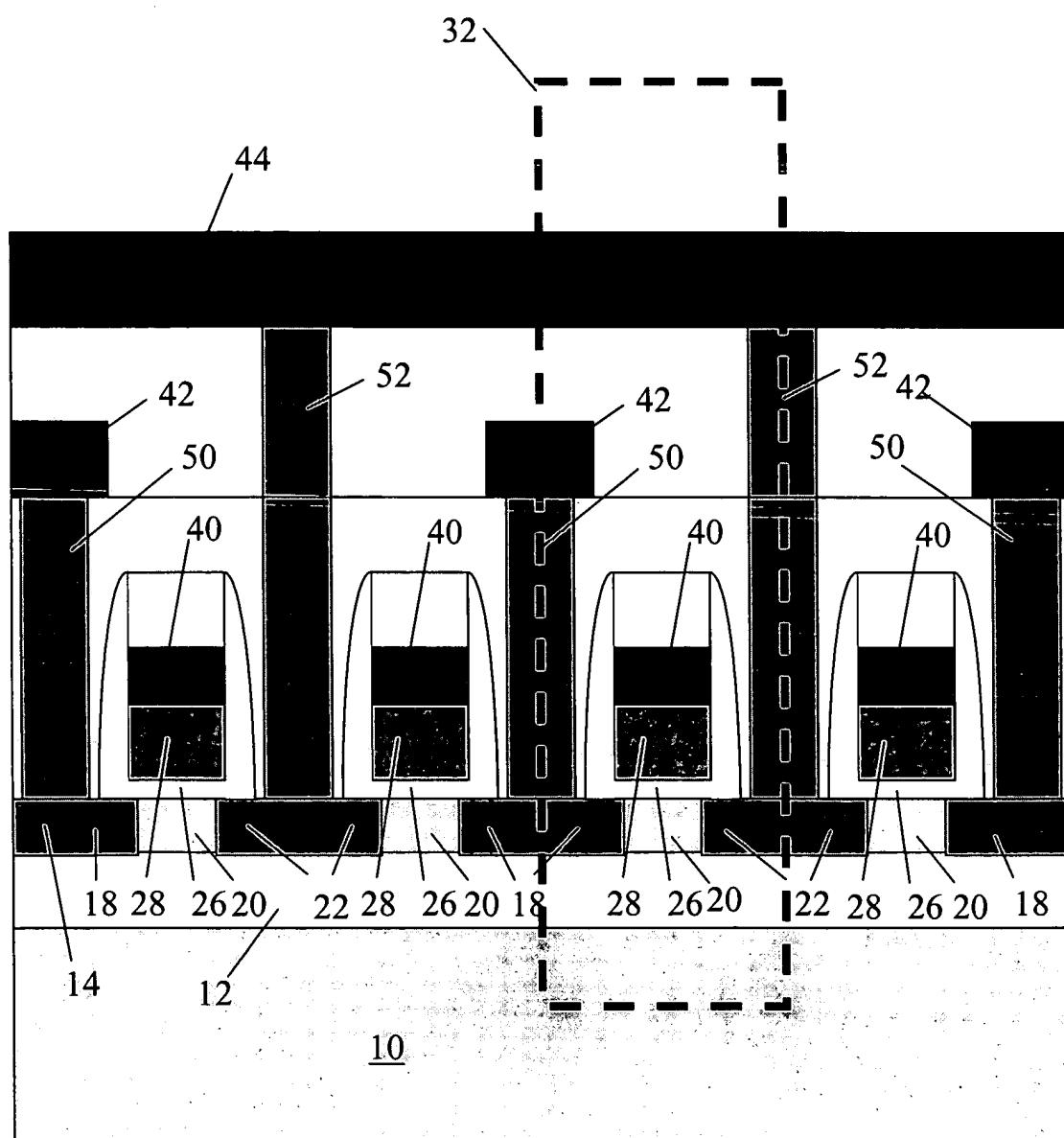


Fig. 17

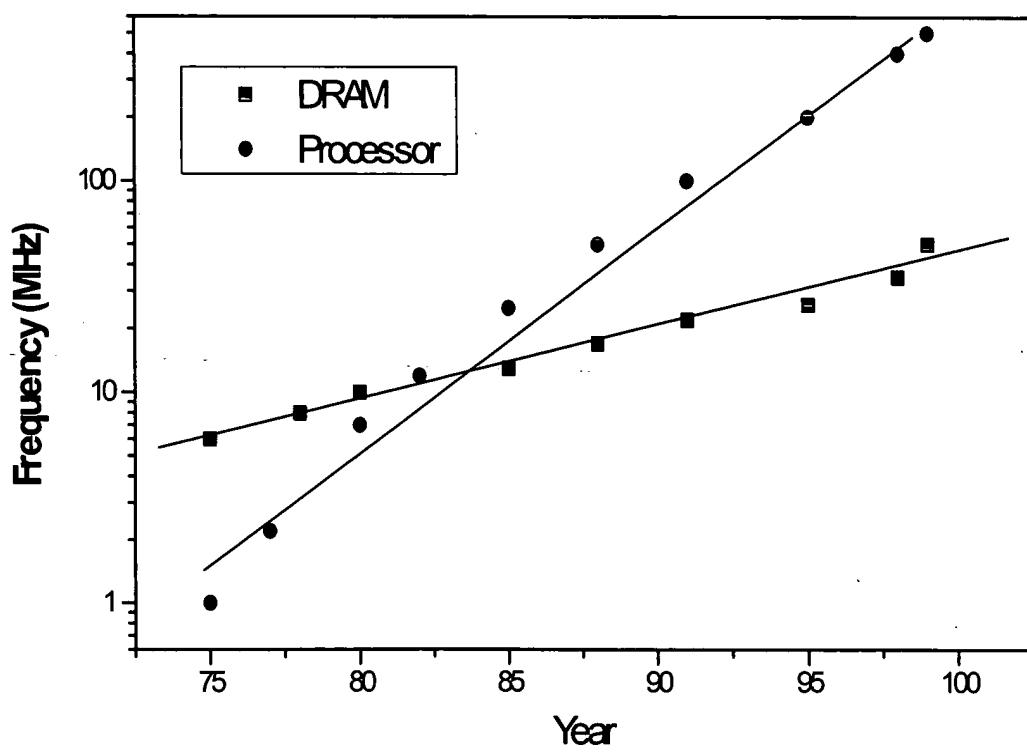


Fig. 18

Schematic of a sensor array

